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10/064,035	06/04/2002	Shyh-Chang Lin	SUNP0006USA	9762

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EXAMINER	
LEE, HWA C	

ART UNIT	PAPER NUMBER
2672	3

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,035	LIN ET AL.	
	Examiner	Art Unit	
	Hwa C Lee	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 June 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan, U.S. Patent Number: 5,691,912, in view of Garnett et al., U.S. Patent Number: 6,516,456, and further in view of Eng, U.S. Patent No.: 6,145,117.

4. In regards to claim 1, Duncan teaches the following:

A method for enabling a user to generate a schematic diagram on a computer system, the computer system comprising a display and an input device, the method comprising: generating a netlist of a schematic diagram, the netlist indicating connectivity of a plurality of components through connection lines;

- Duncan teaches a method and a system of generating a circuit diagram and a state flow diagram using a schematic capture package (Col. 4, lines 50-60). Said method and system comprises generating a schematic diagram, a netlist of the schematic diagram, which describes the connectivity of a plurality of components using connection lines (Col. 7, lines 20-54; Col. 8, line 30 – Col. 9, line 9; and FIG. 5).

providing a normal display mode in which at least a portion of the components are presented on the display, and connection lines corresponding to the displayed components are presented on the display;

- Duncan teaches displaying interactions of components of the state flow diagram and the schematic diagram using interconnect lines (Col. 7, lines 39-46).

5. Duncan does not explicitly teach ***providing a topology display mode in which the at least a portion of the components are presented on the display without the corresponding connection lines***, but Garnett et al. teaches the said limitations.

6. Garnett et al. teaches method and apparatus for selectively viewing interconnections for the desired portion of the schematic diagram (Col. 4, lines 53-67; Col. 5, line 1 – Col. 6, lines 24; Col. 19, lines 7-26; Col. 23, lines 40-55; and FIGS. 18-20). Said selective viewing specifically is ***providing a topology display mode*** as disclosed in the current claim.

7. Garnett et al. also teaches ***wherein the user is capable of switching between the topology display mode and the normal display mode while editing the schematic diagram.***

- Since Garnett et al. teaches selectively viewing the desired interconnections as applied above, Garnett et al. teaches viewing all interconnections (normal view) and viewing only desired interconnections (topology view) (Col. 19, lines 15-58 and FIGS. 8A-D).

8. Duncan and Garnett et al. in combination teach the following:

providing a component selection function that enables a user to utilize the input device to select a particular component;

- Duncan teaches using a commercially available schematic capture package (FIG. 5, No. 20), which comprises a component generator (FIG. 5, No. 30), a schematic editor (FIG. 5, No. 50), a display generator (FIG. 5, No. 60), and a netlist generator (FIG. 5, No. 70), in order to select both schematic components and state flow components for implementing circuit design (Col. 7, line 20 – Col. 9, line 24). Said list of compatible schematic capture package comprises Workview™ 4.1 software package requires a user interface.
- Garnett teaches the method of allowing the designer to enter design information into the electronic design automation (EDA) system using a plurality of input devices (Col. 9, lines 19-38 and FIG. 1). Said EDA system specifically is used to select circuit components when designing circuits.

providing a topology editing function to modify the netlist, the topology editing function enabling the user to utilize the input device to modify the relative positioning, sizing and connectivity of a selected component, wherein the topology editing function is combinable with the topology display mode to enable

the user to edit the relative positioning or sizing of the selected component without viewing the corresponding connection lines;

- As applied above, Duncan teaches editing the arrangement of schematic components and state flow components along with the interconnections of said components using a computer-aided engineering system (CAE) (FIG. 5), which specifically is modifying the netlist as disclosed in the current claim. In addition, the display generator (FIG. 5, No. 60) generates on the video display (FIG. 5, No. 65), the circuit design in order to allow the user to "modify the contents of the circuit design file until it contains a desired circuit design". Thus, said modifying the contents of the circuit design file specifically is ***modifying the relative positioning, size and connectivity of a selected component.***
- Garnett et al. teaches allowing the designer to control the physical attribute values, especially component placement and interconnect routing coordinates using the EDA software (Col. 8, lines 54-67). Controlling said physical attribute values specifically is ***modifying the relative positioning, size and connectivity of a selected component.*** Then the user can choose to display only the desired components and associated interconnections in order to edit only the desired components of the circuit design as applied above.

9. Duncan and Garnett et al. teach ***providing routing of the connection lines modified during the topology editing function according to the netlist*** as applied above, but do not explicitly teach ***automatic pin assignment.*** However, when the

interconnections are provided between the components, said interconnections are made by assigning pins to said interconnections.

10. Eng teaches ***automatic pin assignment***, which is directed to an electronic design automation system (Col. 17, lines 36-45 and FIG. 13, No. 1304).

11. It would have been obvious to one of ordinary skill in the art to take the teachings of Duncan and to add from Garnett et al. the method of selectively viewing the interconnection of only the desired portion of the circuit design in order to avoid the confusion of determining which interconnections belong to which component. Garnett et al. teach avoiding the problem of "rats net" by displaying only the interconnections of desired components. In addition, it would have been obvious to add from Eng, the teachings of optimizing Register-Transfer-Level (RTL) system in order to enhance the existing top-down EDA system by implementing an automatic performance driven design paradigm. Further, all references are directed to editing and displaying circuit designs.

12. In regards to claim 2, the same basis and rationale for claim rejection as applied to claim 1 above are applied.

The method of claim 1 wherein the topology editing function changes the netlist to reflect corresponding changes made by the user to the relative positioning and connectivity of the components.

- Duncan teaches creating a netlist after editing the schematic diagram (FIG. 5, and thus any changes made must be updated in the netlist.

- Garnett et al. teaches changing positioning and connectivity of components, and since a netlist is a list of components and their connectivity, said netlist must be also changed.

13. In regards to claim 3, the same basis and rationale for claim rejection as applied to claims 1-2 are applied.

The method of claim 2 further comprising performing the automatic pin assignment and routing at a time that is after a change is made to the netlist and before entering the normal display mode.

- Both Duncan and Garnett et al. teaches displaying to the user any changes in design in order to allow the user to visualize the circuit design as the editing continues. Thus, all editing of the circuit design is done before displaying the circuit design.

14. In regards to claim 4, Duncan and Garnett et al. in combination teach the following:

The method of claim 1 further comprising utilizing the netlist to classify each connection line according to a driver/load characteristic of the connection line.

- Duncan teaches the schematic editor (FIG. 5, No. 50), which is use to enter the lines connecting the schematic components. In order to connect the components properly, said connecting lines must be sorted based on the input and output edges of the lines, which specifically are driver/load characteristics since all interconnection lines have driver/load characteristics.

- Garnett et al. teaches sorting nets (FIG. 5, No. 136) according to associated components (Col. 17, lines 26-49) and filtering nets (FIG. 5, No. 144 and Col. 17, line 65 – Col. 18, line 11). In addition, Garnet et al. teaches storing net I/O list, which identifies vectored nets and scalar nets (Col. 18, lines 30-36; Col. 20, lines 29-67; and FIG. 10). Said, sorting, filtering, and storing nets specifically are classifying each connection lines as disclosed in the current claim.

15. In regards to claim 5, the same basis and rationale for claim rejection as applied to claims 1 and 4 are applied.

The method of claim 4 further comprising providing an abstract display mode that presents on the display zero or more abstract lines for a first component, each abstract line respectively indicating connectivity of the first component with another component.

- Garnett et al. teaches selecting only the desired component and not displaying the interconnections of said desired components as applied above, which specifically is displaying zero abstract lines. In addition, Garnett et al. teaches using the vector filter block (FIG. 5, No. 144), which filters the display of interconnections between the selected component and associated components. In addition, the user select input block (FIG. 5, No. 138) allows the user to select a component from the sorted list of components, wherein the Auto-select net instance block (FIG. 5, No. 140) automatically selects the next component, which eventually is used to display the desired connectivity only. Further, controlling which nets are displayed specifically reads on the limitation of the current claim.

16. In regards to claim 6, the same basis and rationale for claim rejection as applied to claim 5 are applied.

The method of claim 5 wherein each abstract line indicates a group of one or more connection lines that have common driver/load characteristics.

17. In regards to claim 7, the same basis and rationale for claim rejection as applied to claims 4 and 6 are applied.

The method of claim 6 further comprising providing abstract information on the display for an abstract line, the abstract information indicating the number of driver connection lines and load connection lines in the group of connection lines associated with the abstract line.

- As applied to claim 6, Garnett et al. teaches I/O list of nets, which specifically provides list of driver and load connections, which are list of components that are upstream and downstream of said net) for each net.

18. In regards to claim 8, the same basis and rationale for claim rejection as applied to claim 5 are applied.

The method of claim 5 wherein the first component is the user-selected component.

- Garnett et al. clearly teaches using the user input block (FIG. 5, No.138) to allow the user to select a desired component first, and then automatically placing the rest of components along with the interconnection lines.

19. In regards to claim 9, the same basis and rationale for claim rejection as applied to claims 1 and 5 above.

The method of claim 5 wherein the abstract display mode is combinable with the topology display mode.

- Garnett et al. teaches controlling which nets to display, and thus is combining a plurality of display modes.

20. In regards to claim 10, the same basis and rationale for claim rejection as applied to claims 1-4 are applied.

The method of claim 4 wherein the automatic pin assignment and routing of the connection lines comprises: grouping together connection lines having common driver/load characteristics to form one or more routing groups; for each routing group, utilizing a router to generate a routing line that routes between two components; and splitting the routing line to provide a respective route and pin assignment for each connection line in the routing group.

21. In regards to claim 11, the same basis and rationale for claim rejection as applied to claims 6 and 10 area applied.

The method of claim 10 wherein each connection line in each routing group shares the same driver component and the same load component.

22. In regards to claim 12, the same basis and rationale for claim rejection as applied to claims 2-3 and 10 are applied.

The method of claim 10 wherein the netlist is modified to reflect the routing and pin assignment performed for each connection line.

23. In regards to claim 13, the same basis and rationale for claim rejection as applied to claim 1 are applied.

The method of claim 1 wherein the topology editing function comprises a central template auto-arrange function that automatically arranges other components around a user-selected component according to the relative connectivity of the other components with the user-selected component.

- As applied to claim 1 above, Garnett et al. clearly teaches using a combination of manual and automated component placement during the circuit design. Once the user manually places some of the components and associated interconnections, the rest of the components are laid out using automated software. Garnett et al. also discloses said method as being a standard practice in the prior art (Col. 4, lines 25-36 and Col. 17, 26-49).

24. In regards to claim 14, Garnett et al. teaches ***wherein the topology editing function comprises a fan-in auto-arrange function that automatically arranges other components with respect to a user-selected component according to fan-in connectivity of the other components with the user-selected component.***

- Garnett et al. teaches performing the net sort as applied to claim 4 above, wherein the first component is manually place by the user. Then the rest of the components are automatically place based on the direction for the said placement of further components (Col. 17, lines 26-41; Col. 18, lines 43-72 and FIG. 7). Said direction reads on both ***fan-in*** and ***fan-out*** functions.

25. In regards to claim 15, the same basis and rationale for claim rejection as applied to claims 13-14 are applied.

The method of claim 14 wherein the user-selected component is placed in a right-most position with respect to the other components.

- As applied to claims 13, Garrett et al. teaches manually placing components, wherein the user controls the placement of the components, and thus Garret et al. teaches placing the user-selected component in a right most position. In addition, since fan-in refers to the selected component being driven by 'up-stream' components, said selected component must be placed in a left most position, wherein the standard circuit flow is from left to right.

26. In regards to claim 16, the same basis and rationale for claim rejection as applied to claim 13 are applied. In addition, Garnett et al. teaches ***fan-out auto-arrange function that automatically arranges other components with respect to a user-selected component according to fan-out connectivity of the other components with the user-selected component.***

- Transitive fan-out refers to all components 'down-stream' of the selected components, wherein the selected component 'drives' all 'down-stream' components (Col. 21, lines 1-65 and FIG. 11).

27. In regards to claim 17, the same basis and rationale for claim rejection as applied to claims 13 and 16 are applied.

The method of claim 16 wherein the user-selected component is placed in a left-most position with respect to the other components.

- As applied to claim 13, Garrett et al. teaches manually placing components, wherein the user controls the placement of the components, and thus Garret et

al. teaches placing the user-selected component in a left most position. In addition, since fan-out refers to the selected component driving all the receiving components, said selected component must be placed in a left most position, wherein the standard circuit flow is from left to right.

28. In regards to claim 18, the same basis and rationale for claim rejection as applied to claims 14-17 are applied. Said ***fan-in*** and ***fan-out auto-arrange functions*** specifically are ***path auto-arrange functions***. In addition, Garnett et al. teaches circuit component arrangement based on data path (Col. 19, lines 26-38).

The method of claim 1 wherein the topology editing function comprises a path auto-arrange function that automatically arranges user-selected components into a path structure, and arranges other components around the user-selected components according to the relative connectivity of the other components with the user-selected components.

29. In regards to claim 19, the same basis and rationale for claim rejection as applied to claims 1, 7, 13-14 and 16 are applied.

The method of claim 1 further comprising: providing a line selection function that enables the user to utilize the input device to select a particular connection line; and providing a bus auto-arrange function that automatically arranges the components around a user-selected connection line according to the relative connectivity of the components with the user-selected connection line.

- Duncan teaches the schematic editor, wherein the building blocks of the circuit design is inputted by the user, and thus reads on user input device for selecting particular components and connections lines.
- Garnett et al. teaches sorting nets, wherein the nets (connection lines) must be selected to be sorted. In addition, the I/O list of net names describes the components, which are connected to each net. Thus, said I/O list provides information about components that are connected by each net and is used to arrange the components of the circuit design.

30. In regards to claim 20, Duncan and Garnett et al. teach the following:

A computer system comprising a processor and memory, the memory holding a program adapted to perform the method of claim 1 and executable by the processor.

- Duncan teaches an IBM computer with a processor and RAM for running the necessary software (Col. 8, lines 17-23).
- Garnett et al. teaches a computer system comprising a processor and a plurality of memory, wherein the source code and software for controlling the operations of the system are stored (Col. 8, lines 16-28 and Col. 9, lines 1-38).

31. In regards to claim 21, the same basis and rationale for claim rejection as applied to claim 20 are applied.

A computer readable media containing data that is adapted to be extractable for providing the program of claim 20.

- Duncan teaches a hard-disk memory, which specifically is a computer readable media.
- Garnett et al. teaches said memory of claim 20, which comprise a plurality of computer readable media (e.g. magnetic disk, optical disk, and magnetic tape).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hwa C Lee whose telephone number is 703-305-8987. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 703-305-3885. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hwa C Lee
Examiner
Art Unit 2672

JOSEPH MANCUSO
PRIMARY EXAMINER

HCL

04/16/04